ALU signal [4:0]			
000	0000000	ADD	00000
000	0100000	SUB	10000
001	0000000	SLL	00001
010	0000000	SLT	00010
011	0000000	SLTU	00011
100	0000000	XOR	00100
101	0000000	SRL	00101
101	0100000	SRA	10101
110	0000000	OR	00110
111	0000000	AND	00111
000	0000001	MUL	01000
001	0000001	MULH	01001
010	0000001	MULHSU	01010
011	0000001	MULHU	01011
100	0000001	DIV	01100
101	0000001	REM	01101
111	0000001	REMU	01111
xxx	xxxxxx	FWD	11xxx

Main mem read [3:0]			
0000011	000	LB	1000
0000011	001	LH	1001
0000011	010	LW	1010
0000011	100	LBU	1100
0000011	101	LHU	1101

Main mem write [2:0]			
0100011	000	SB	100
0100011	001	SH	101
0100011	010	SW	110

oparand 1 MUX	
1	PC
0	REG_DATA1

oparand 2 MUX	
1	immediate
0	REG_DATA2

Reg write select MUX [1:0]	
00	PC+4
01	ALU result
10	MEM_READ

Immidiate Select [3:0]	
TYPE 1	u000
TYPE 2	u001
TYPE 3	u010
TYPE 4	u011
TYPE 5	u100
TYPE 6	u101